

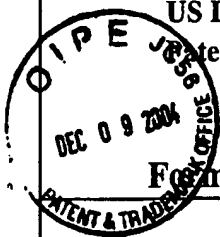
 <p>US Department of Commerce Patent and Trademark Office</p> <p>Form PTO-1449 (Modified)</p>				Atty. Docket No.: 42390.P5193C		Application No.: 09/852,217	
				Applicant: Abdallah et al.			
				Filing Date: May 8, 2001			
US Patent Documents							
Examiner's Initials	Date	Document Number	Name	Class	Sub- Class	Filing Date	
EC	07/31/90	4,945,479	Rusterholz et al.	712	3		
EC	11/20/90	4,972,362	Elkind et al.	708	632		
EC	09/10/91	5,047,975	Patti et al.	708	706		
EC	01/14/92	5,081,698	Kohn	345	422		
EC	11/30/92	5,161,247	Murakami et al.	712	36		
EC	02/23/93	5,189,636	Patti et al.	708	706		
EC	07/05/94	5,327,369	Ashkenazi	708	710		
EC	02/14/95	5,390,135	Lee et al.	708	518		
EC	05/07/96	5,515,520	Hatta et al.	708	550		
EC	11/26/96	5,579,253	Lee et al.	708	625		
EC	12/31/96	5,590,365	Ide et al.	712	218		
EC	04/21/98	5,742,840	Hansen et al.	712	210		
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EC	09/15/98	5,809,321	Hansen et al.	712	1		
EC	10/13/98	5,822,603	Hansen et al.	712	1		
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EC	12/21/99	6,006,318	Hansen et al.	712	28		
EC	09/25/01	6,295,599	Hansen et al.	712	32		
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EC	06/24/03	6,584,482	Hansen et al.	708	523		
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EC	04/20/04	6,725,356	Hansen et al.	712	210		
Foreign Patent Documents							
Examiner's Initials	Date	Document Number	Country	Class	Sub- Class	Translation	
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)							
Examiner <i>Wie</i>			Date Considered <i>2/16/05</i>				

Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw a line through the citation if not in conformance and not considered. Include a copy of this form with the next communication to the applicant

 <p style="margin: 0;">US Department of Commerce Patent and Trademark Office Form PTO-1449 (Modified)</p>		Atty. Docket No.: 042390.P5193C		Application No.: 09/852,217		
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Examiner's Initials	Date	Document Number	Name	Class	Sub- Class	Filing Date
Foreign Patent Documents						
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Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)						
EC		Santoro, Mark; Design and Clocking of VLSI Multipliers. Technical Report No. CSL -TR-89-397, October 1989. Pages i-xii and 1-118.				
EC		Santoro, Mark, et al.; SPIM: A Pipelined 64X64 bit Iterative Multiplier, IEEE Journal of Solid -State Circuits, Vol. 24, No. 2, April 1989. Pages 487-493.				
EC		Santoro, Mark, et al.; SESSION II: HIGH-SPEED MICROPROCESSOR. WAM 2.6: A Piplelined 64X64b Iterative Array Multiplier. 1988 IEEE International Solid State Circuits Conference . Pages 36-37 and 290.				
EC		BIT Preliminary, Bipolar Integrated Technology, Inc. B3110/B3120;B2110/B2120 Floating Point Chip Set. Pages 1-40.				
EC		Eklind, Bob, et al. A SUB 10 nS Bipolar 64 Bit Integrated/Floating Point Processor Implemented On Two Circuits. IEEE 1987 BCTM, pages 101- 104				
EC		Leibowitz, Bob; et al., System Design; ECL gains ground in battle against CMOS. Computer Design; April 1, 1987. Pages 91-95.				
EC		IBM. TBD: Double Speed, Single Precision Vector Register Organization Using Double Port Chips. Feb. 1981. Pp.1-6.				
EC		Farmwald, P. Michael; High Bandwidth Evaluation of Elementary Functions, S-1 Project. IEEE 1981. Pages 139 - 142.				
EC		Farmwald, P. Michael; On the Design of High Performance Digital Arithmetic Units. UCRL-53190. August 1981. Pages i-vii and 1-95.				
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Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

EC	Ide, et al.; A 320-MFLOPS CMOS Floating-Point Processing Unit for Superscalar Processors. IEEE Journal of Solid State Circuits, Vol. 28, No. 3, March 1993. Pages 352 - 361.
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EC	Lee, Ruby B.; Accelerating Multimedia with Enhanced Microprocessors. Hewlett-Packard. IEEE Micro, April 1995. Pages 22-32.
EC	Lee, Ruby B.; Realtime MPEG Video via Software Decompression on a PA-RISC Processor. 1995 IEEE, pages 186-192.
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EC	Undy, Steve, et al.; A Low-Cost Graphics and Multimedia Workstation Chip Set. April 1994, IEEE micro, pages 10 - 22.

Examiner

E. H.

Date Considered

2/16 /05

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